

WHAT IS CLAIMED IS:

1                   1.       A digital system integrated on a semiconductor chip, comprising:  
2                   one or more first bus masters coupled to a first bus in a first clock domain;  
3                   a programmable logic device coupled to a second bus in a second clock  
4 domain;  
5                   a first bridge coupled between the first and second buses operable to de-  
6 couple the first clock domain from the second clock domain.

1                   2.       The system of claim 1, wherein one of the first bus masters  
2 comprises a central processing unit.

1                   3.       The system of claim 1, wherein the one or more first bus masters  
2 are configured to communicate with the one or more second bus slaves coupled to the  
3 second bus, via the first bridge.

1                   4.       The system of claim 1, wherein the programmable logic device  
2 comprises a second bus master.

1                   5.       The system of claim 4, further comprising a second bus bridge  
2 coupled between the second bus and the second bus master.

1                   6.       The system of claim 1, further comprising a plurality of second bus  
2 masters coupled to the second bus.

1                   7.       A digital system on a semiconductor chip, comprising:  
2 a central processing unit (CPU) coupled to a first bus;  
3 a programmable logic device (PLD) coupled to a second bus; and  
4 a bus bridge coupled between the first and second buses.

1                   8.       The digital system of claim 7, wherein the first bus operates within  
2 a first clock domain and the second bus operates within a second clock domain.

1                   9.       The digital system of claim 8, wherein the first clock domain is  
2 characterized by a first clock frequency that is greater than a second clock frequency  
3 characteristic of the second clock domain.

1                   8.     The digital system of claim 7, wherein the first bus operates  
2     within a first clock domain and the second bus operates within a second clock domain.

1                   9.     The digital system of claim 8, wherein the first clock domain is  
2     characterized by a first clock frequency that is greater than a second clock frequency  
3     characteristic of the second clock domain.

1                   10.    The digital system of claim 8, wherein either or both of the first  
2     clock frequency and second clock frequency are programmable.

1                   11.    A digital system on a semiconductor chip, comprising:  
2                   a central processing unit (CPU) coupled to a first bus in a first clock  
3     domain defined by a first bus clock frequency;  
4                   a plurality of electronic devices coupled to a second bus in a second  
5     clock domain defined by a second bus clock frequency;  
6                   a bus bridge coupled between the first and second buses and operable to  
7     allow communication between the CPU at the first bus clock frequency and one of the  
8     plurality of electronic devices at the second bus clock frequency;  
9                   a programmable logic device (PLD) coupled to a third bus in a third  
10    clock domain; and  
11                  a PLD bridge coupled between the second and third buses.

1                   12.    A device comprising:  
2                   a first circuit operable in a first clock domain;  
3                   a first communication media coupled to the first circuit and configured to  
4     transfer information;  
5                   a second circuit operable in a second clock domain;

6           a second communication media coupled to the second circuit and the first  
7 communication media, wherein the second communication media configured to  
8 transfer information; and  
9           a communication circuit coupled to the first and second communication  
10 medium and configured to provide communication between the first and second  
11 circuits.

1           13.    The device of claim 12, wherein the device includes a plurality of  
2 circuits deposited on an integrated circuit.

1           14.    The device of claim 12, wherein the first circuit is a processor.

1           15.    The device of claim 12, wherein the first clock domain provides a first  
2 programmable clock frequency.

1           16.    The device of claim 15, wherein the frequency of the first  
2 programmable clock frequency can be selectively programmed.

1           17.    The device of claim 12, wherein the first communication media is a bus.

1           18.    The device of claim 12, wherein the information includes data.

1           19.    The device of claim 12, wherein the information includes control  
2 signals.

1           20.    The device of claim 12, wherein the second circuit is a programmable  
2 logic device.

1           21.    The device of claim 20, wherein the programmable logic device further  
2 includes:

3 a plurality of logic cells having at least one programmable circuit arranged in a  
4 multiple dimensional array; and  
5 at least one interconnector coupled to the plurality of the logic cells and  
6 configured to transfer information between the plurality of the logic cells.

1 22. The device of claim 12, wherein the second clock domain includes a  
2 second programmable clock frequency.

1 23. The device of claim 22, wherein the first programmable clock frequency  
2 has the same frequency of the second programmable clock frequency.

1 24. The device of claim 12, wherein the communication circuit is a bus  
2 bridge.

1 25. The device of claim 24, wherein the bus bridge transfers the information  
2 between the first and second clock domains.